1. Device Overview

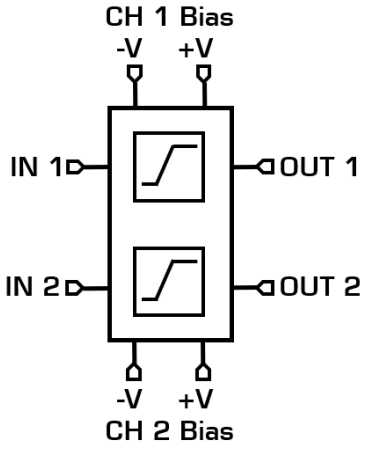
1.1 General Description

The DLM-10SM is a tunable, dual channel GaAs Schottky diode signal limiter featuring excellent IP3, insertion loss, and return loss. The limiting level is adjustable with an off-chip bias network, and the two channels can be used for differential or single-ended signals. The DLM-10SM is available in a lead-free, RoHS compliant QFN surface mount package and is compatible with standard leaded and lead-free PCB reflow soldering processes. The DLM-10SM is a superior alternative to discrete diode limiting options.

1.2 Features

- Industry leading IP3, low insertion loss, and return loss
- Adjustable limiting level with off-chip bias network
- Single channel differential/Dual channel single ended
- RoHS compliant

1.3 Functional Block Diagram



1.4 Part Ordering Options[1]

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
DLM-10SM	3x3 mm QFN	SM	**RoHS**	Active	EAR99
EVAL-DLM-10	Connectorized Evaluation Fixture	Eval		Active	EAR99

[1] Refer to our website for a list of definitions for terminology presented in this table.

Table of Contents

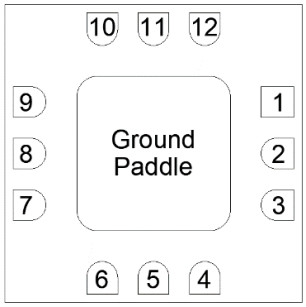
Revision History

Revision Code	Revision Date	Comment
-	January 2017	Initial Release
A	May 2019	Added Max Power Handling, Updated ESD rating
B	September 2019	Added isolation plot
C	October 2021	Corrected Block Diagram, Updated Port Functions, Typical Performance Plots, Added Insertion Loss vs Bias, Power Transfer vs Frequency, IP3 vs Bias, EVAL Package Weight, EVAL Package Outline

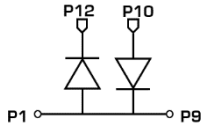
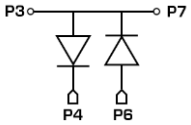
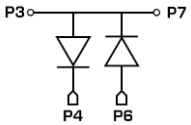
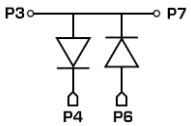
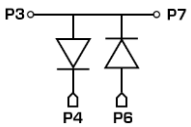
2. Port Configurations and Functions

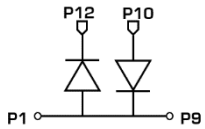
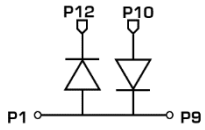
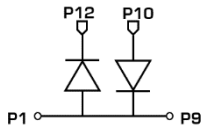
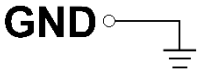
2.1 Port Diagram

A bottom-up view of the DLM-10SM's SM package outline drawing is shown below. The DLM-10SM has the input and output ports given in Port Functions.

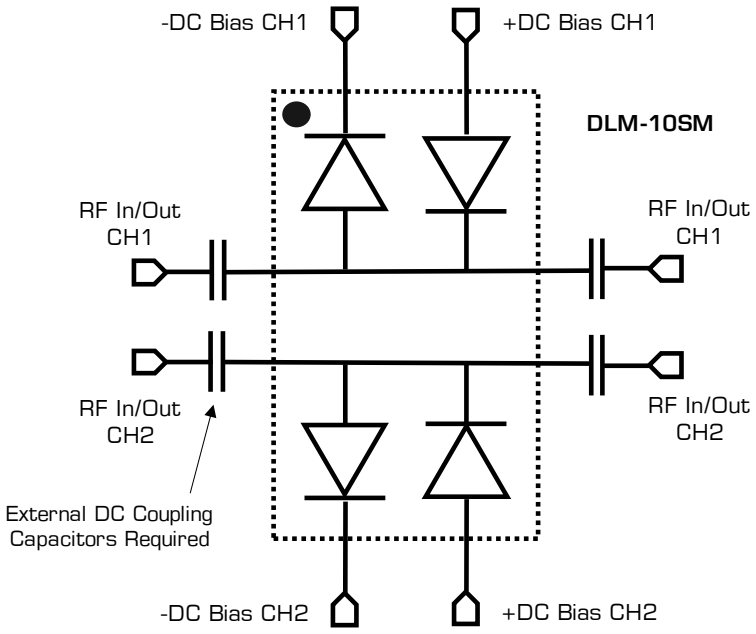


2.2 Port Functions

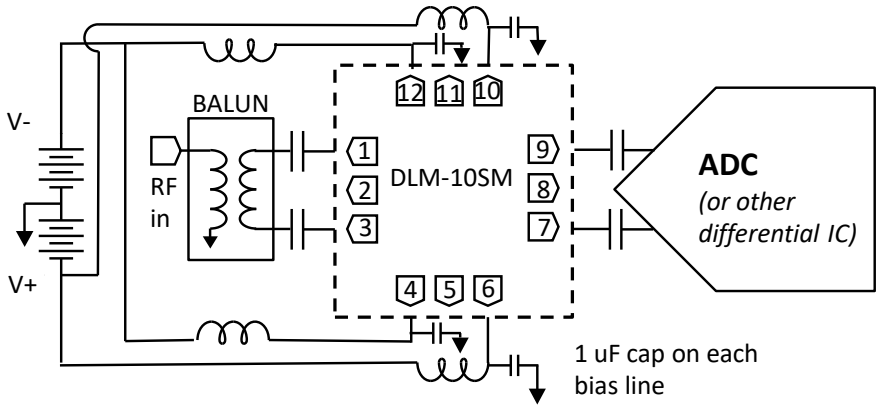
Pad	Function	Description	Equivalent Circuit for Package
1	RF In/Out CH 1	Pad 1 is DC short to pad 9 and diode connected to pins 10 and 12.	
3	RF In/Out CH 2	Pad 3 is DC short to pad 7 and diode connected to pins 4 and 6.	
4	-DC Bias CH 2	Pad 4 is diode connected to pad 3 and pad 7.	
6	+DC Bias CH 2	Pad 6 is diode connected to pad 3 and pad 7.	
7	RF Out/In CH 2	Pad 7 is DC short to pad 3 and diode connected to pins 4 and 6.	

9	RF Out/In CH 1	Pad 9 is DC short to pad 1 and diode connected to pins 10 and 12.	
10	+DC Bias CH 1	Pad 10 is diode connected to pad 1 and pad 9.	
12	-DC Bias CH 1	Pad 12 is diode connected to pad 1 and pad 9.	
GND	Ground	Ground is provided through ground paddle.	

2.3 Block Diagram



2.4 Example Application Circuit



Differential/Two Channel Operation – The two limiting channels are not coupled together, so the device can be used as a single channel, two channel, or differential limiter. If the second channel is not used, it should be connected to RF ground.

Grounded Operation – Pins 4,6, 10, and 12 can be connected directly to RF/DC ground for ease of use. This will give a limiting level of around 7 dBm. If a higher or lower limiting level is desired, please see biased operation.

Biased Operation – For lower limiting levels, the internal diodes can be slightly forward biased to decrease the threshold voltage. A positive voltage should be applied to Pins 10 and 6, and an equal negative voltage should be applied to pins 4 and 12 for symmetric limiting. To increase the limiting threshold, the diodes should be reversed biased. This means that a negative voltage should be applied to pins 10 and 6, and an equivalent positive voltage should be applied to pins 4 and 12.

Biasing Circuitry – A voltage/current source that can both source and sink current must be used. Many voltage leveling circuits can only supply current to set a *minimum* voltage. In this case the signal will cause the diodes to self-bias in limiting operation, increasing the bias threshold. The bias supply must be able to sink current to prevent self-biasing. A low impedance RF ground must be provided by bypass capacitors to ground as close as possible to the bias pins. High frequency bypass capacitors are included on chip, so only low frequency (~1uF) capacitors are necessary. The DC power supply should be decoupled from the limiter circuit through an RF choke and decoupling capacitors if necessary to eliminate power supply noise.

3. Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Units
Forward Bias Voltage	0.5	V
Reverse Bias Voltage	4	V
Maximum Input Power	+27	dBm
Operating Temperature	-55 to +85	°C
Storage Temperature	-65 to +150	°C

3.2 Package Information

Parameter	Details	Rating
ESD	Human Body Model (HBM), per MIL-STD-750, Method 1020	1A
Weight	Eval Package	24.3 g

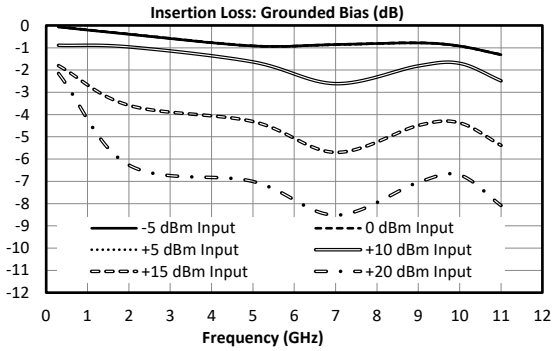
3.3 Electrical Specifications

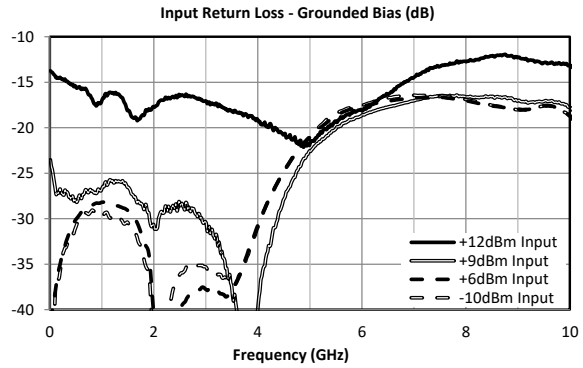
The electrical specifications apply at T_A=+25°C in a 50Ω system. Typical data shown is for the connectorized EVAL package unless otherwise specified. Linear Specifications valid for input power up to the 0.1dB compression point. See page 5 for P0.1dB graph.

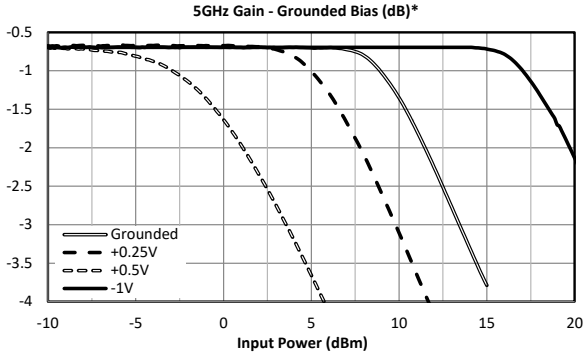
Min and Max limits are guaranteed at T_A=+25°C.

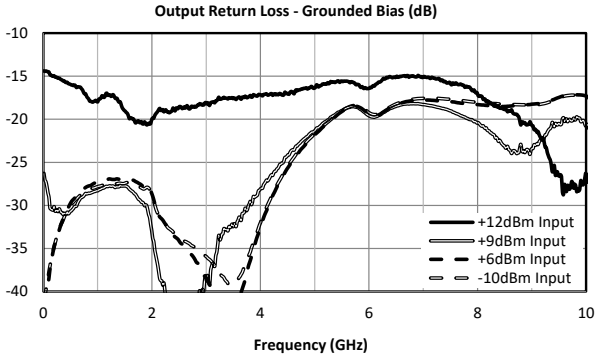
Parameter	Test Conditions	Input Power (dBm)	Min	Typical	Max	Units
Insertion Loss, Grounded Bias	DC – 10GHz	-10		0.75	1.5	dB
		+10		1.4		
		+15		3.75		
Input 1dB Compression, Grounded Bias (dBm)				10		
Return Loss, Grounded Bias		-10 to +9		20		dB
		+12		15		
Group Delay				260		ps

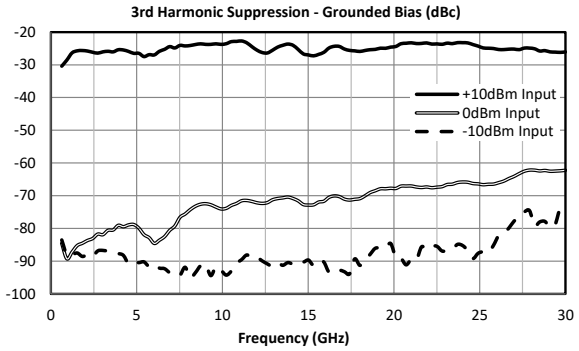
3.4 Typical Performance Plots

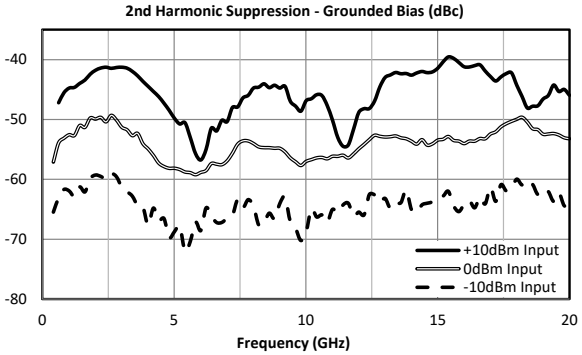


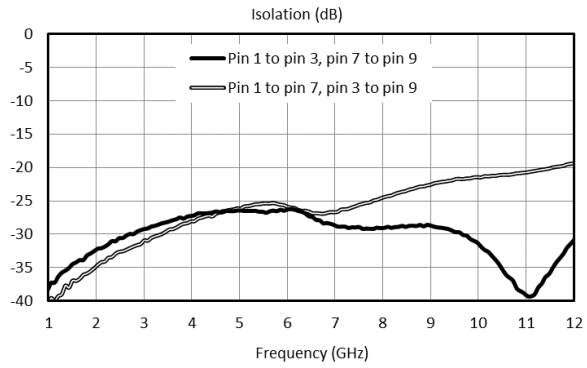


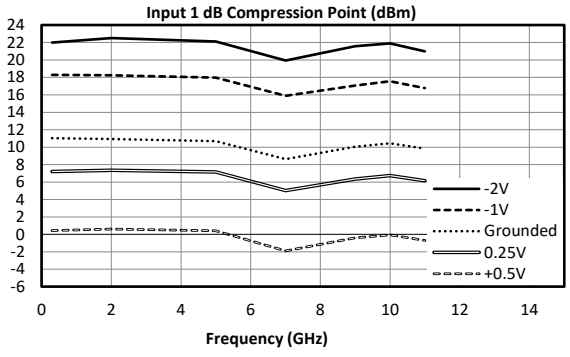




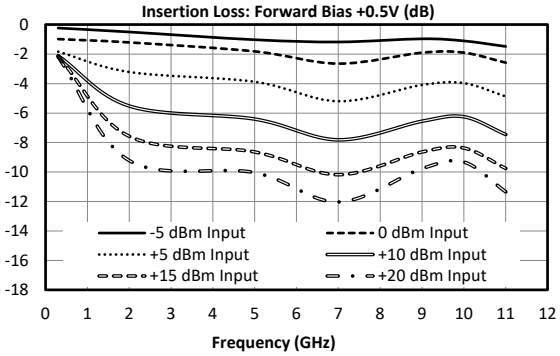


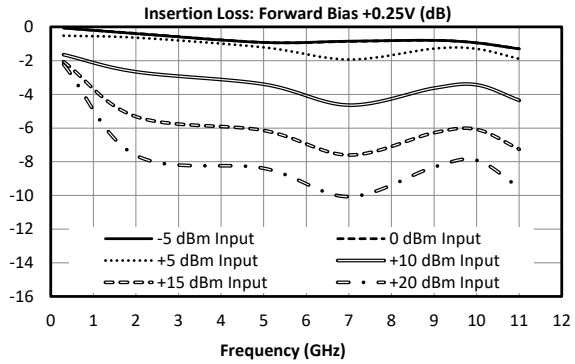


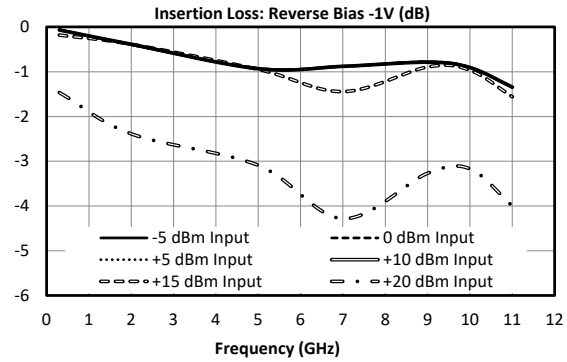


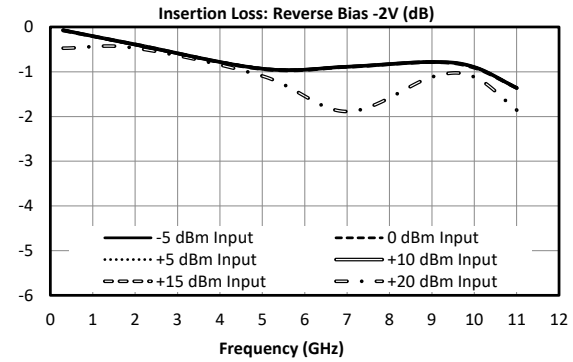


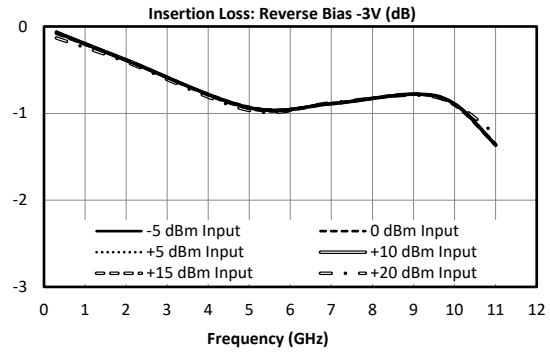
3.4.1 Insertion Loss vs Bias

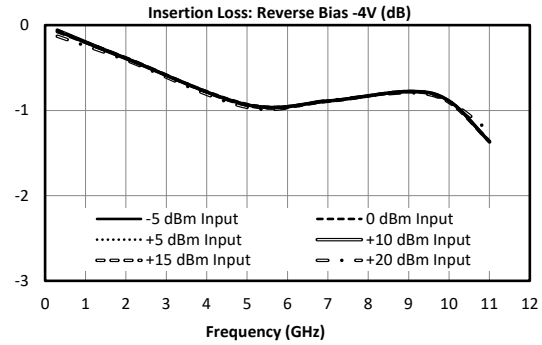




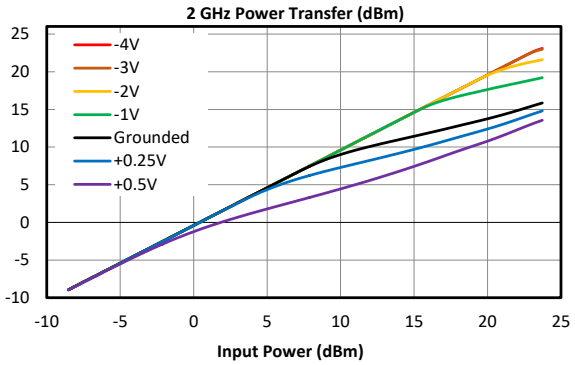


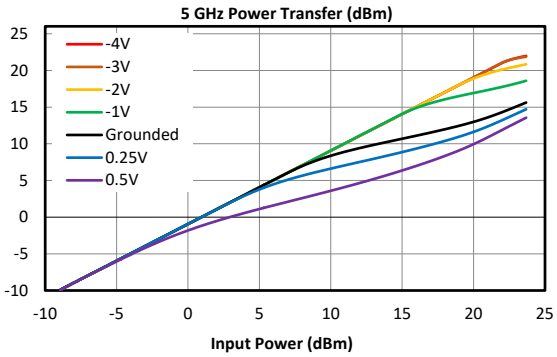


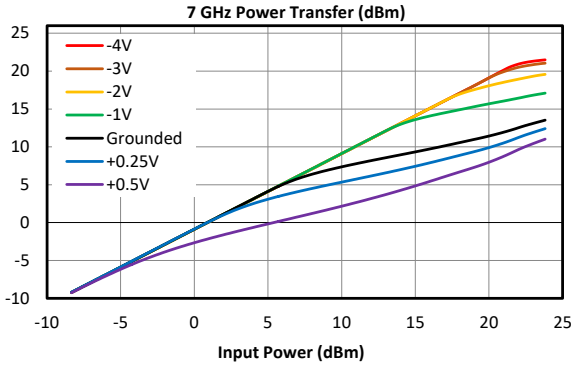


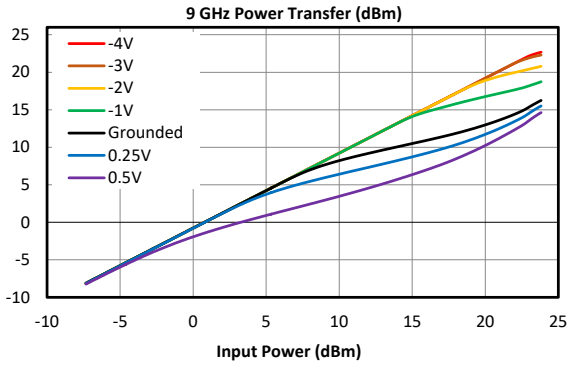


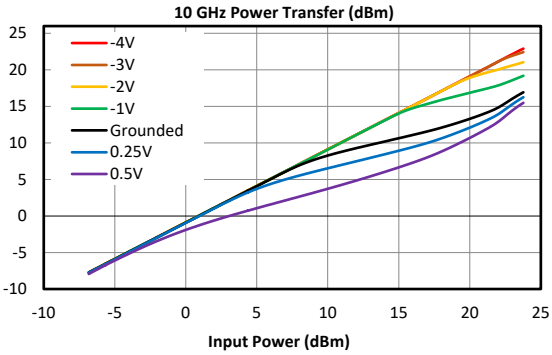
3.4.2 Power Transfer vs Frequency



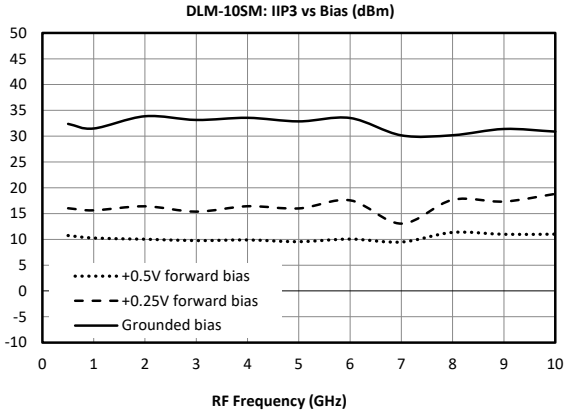


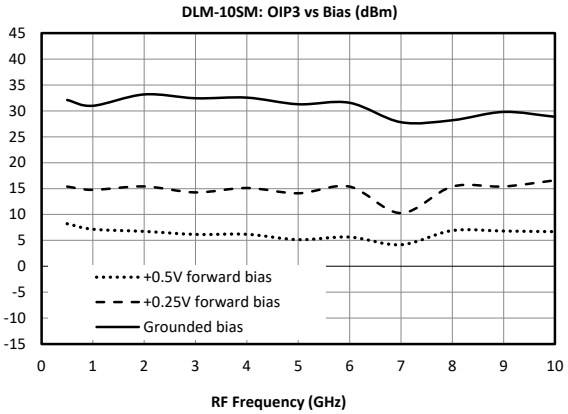






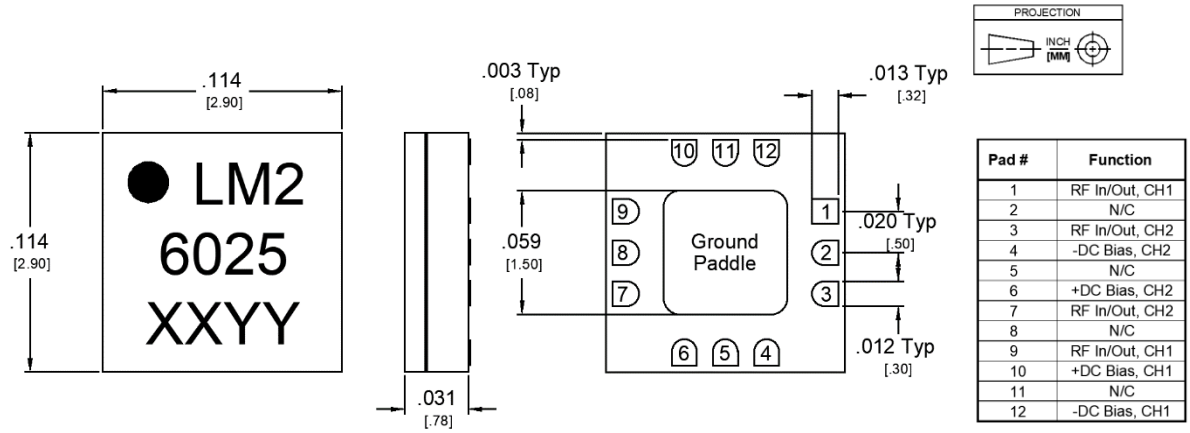
3.4.3 IP3 vs Bias





4. Mechanical Data

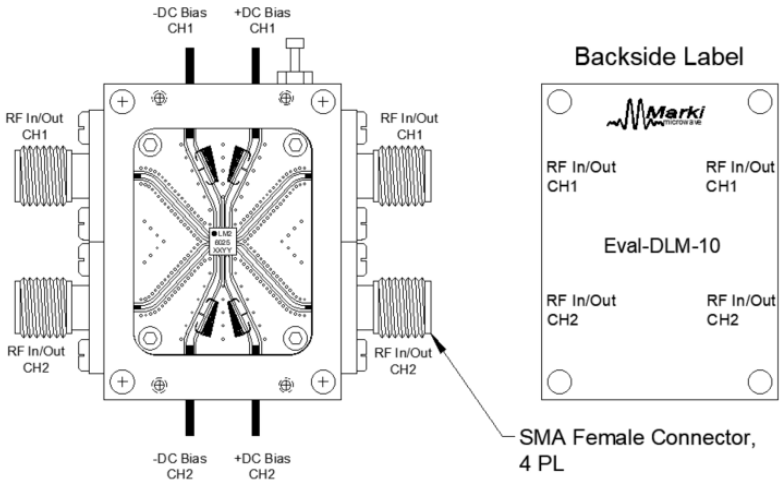
4.1 SM Package Outline Drawing



Pad #	Function
1	RF In/Out, CH1
2	N/C
3	RF In/Out, CH2
4	-DC Bias, CH2
5	N/C
6	+DC Bias, CH2
7	RF In/Out, CH2
8	N/C
9	RF In/Out, CH1
10	+DC Bias, CH1
11	N/C
12	-DC Bias, CH1

1. Substrate material is ceramic.
2. I/O Leads and Ground Paddle are 2.0 um MAX Au over 1.3 um Ni.
3. All unconnected pads should be connected to PCB RF ground.

4.2 EVAL Package Outline Drawing



Unless otherwise specified, dimensions are in inches. Tolerances are:

.XX ± .02
.XXX ±.005